Application Note 3071
Internal Test Registers for the DS31256

www.maxim-ic.com

OVERVIEW

The DS31256 HDLC controller has some registers that are for internal test use only (see Table 1). The user should avoid using them.

Table 1. Test Registers

ADDRESS (h)	VALUE (h)
0050 (Test Register)	0000
04F0 to 04FF	0000
07FD to 07FF	0000
08FD to 08FF	0000
09F8 to 09FF	0000

All test registers in DS31256 are 16 bits and set to 0 with the hardware or software reset. Only the description of test register at address 0050 is shown in the data sheet. All other test registers are hidden registers and for internal test only (not shown in the data sheet).

OFFSET/ADDRESS	ACRONYM	REGISTER NAME	DATA SHEET SECTION
0050	TEST	Test Register	5.4

Test register bit 0 is used by the factory-test (FT) mode to place the DS31256 in the test mode. For normal device operation, this bit should be set to 0 whenever this register is written to. Setting this bit places the RAMs into a low-power standby mode.

Bits 1 to 15 is for internal (Dallas Semiconductor) test use only, not user test-mode controls. Values of these bits should always be 0. If any of these bits are set to 1, the device does not function properly.

DS31256 INFORMATION

For more information about the DS31256, refer to the data sheet, which is available on our website at www.maxim-ic.com/DS31256.

CONCLUSION

This application note has listed the internal test registers for the DS31256 and explained why the user should avoid using these registers.

If you have further questions about our HDLC controller products, please contact the Telecommunication Applications support team via email at telecom.support@dalsemi.com, or call 972-371-6555.